EXHIBIT 14

Exhibit 14: U.S. Patent No. 6,871,264

Claim 1	Identification
1[pre]. A processor integrated circuit capable of executing more than one instruction stream comprising:	To the extent the preamble is limiting, SAP provides a processor integrated circuit capable of executing more than one instruction stream. For example, *see*:  Source: https://www.youtube.com/watch?v=ECHhuvuiNzs (Nov. 8, 2021)

Claim 1	Identification

AMD EPYC CPUs Now Power SAP Applications Hosted on Google Cloud

SANTA CLARA, Calif., July 11, 2023 (GLOBE NEWSWIRE) -- Today, AMD (NASDAQ: AMD) announced that SAP has chosen AMD EPYC™ processor-powered Google Cloud N2D virtual machines (VMs) to run its cloud ERP delivery operations for RISE with SAP; further increasing adoption of AMD EPYC for cloud-based workloads. As enterprises look toward digital modernization, many are adopting cloud-first architectures to complement their on-premises data centers. AMD, Google Cloud and SAP can help customers achieve their most stringent performance goals while delivering on energy efficiency, scalability and resource utilization needs.

"As part of our RISE with SAP initiative, we have made a strategic decision to add AMD EPYC processor powered N2D instances in Google Cloud to run mission critical workloads for our enterprise cloud customers." said Lalit Patil, CTO, SAP Enterprise Cloud Services, SAP SE. "Our engineering collaboration with AMD and Google Cloud can result in an increase in performance and performance-per-dollar over comparable instances."

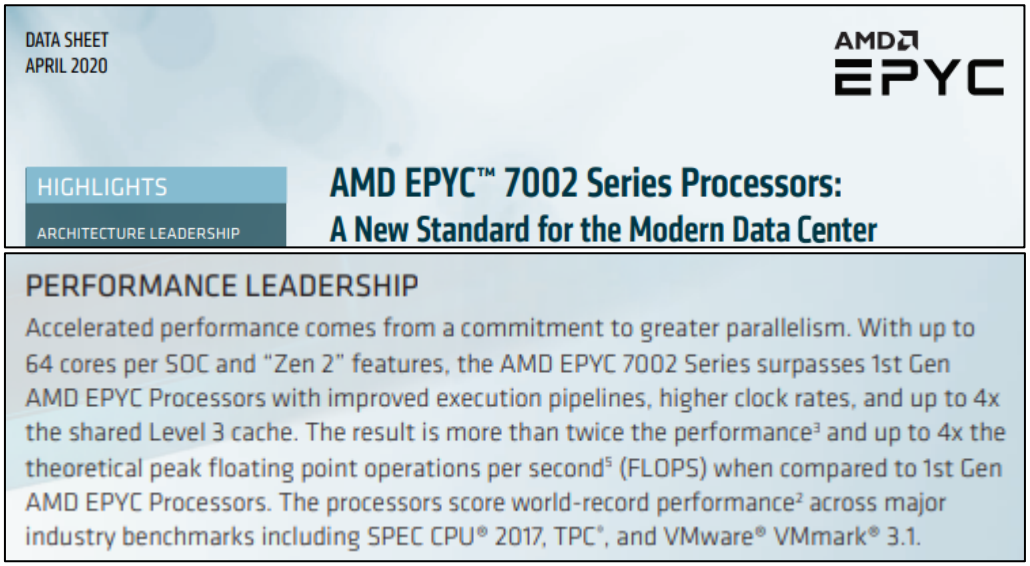
Source: https://www.amd.com/en/newsroom/press-releases/2023-7-11-amd-epyc-cpus-now-power-sap-applications-hosted-on.html

— What is the difference between SAP S/4HANA Cloud, private edition and RISE with SAP?

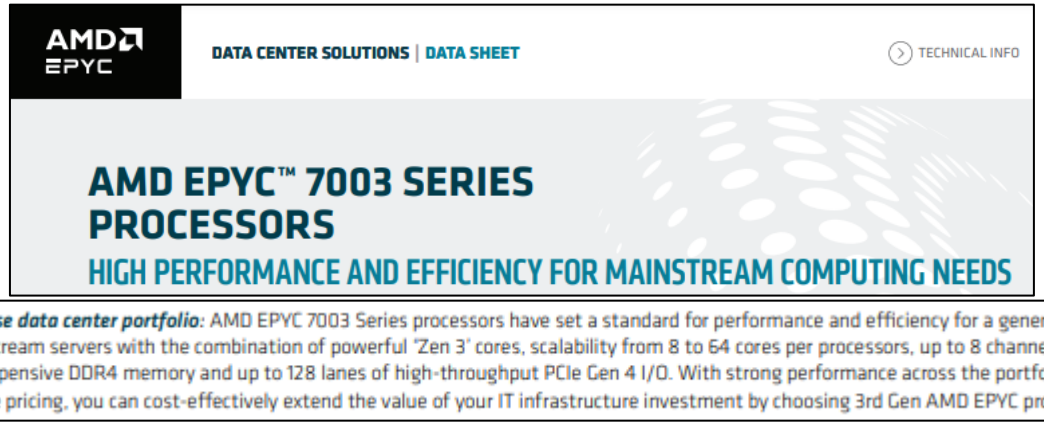
SAP S/4HANA Cloud, private edition is the cloud ERP at the heart of RISE with SAP. RISE with SAP bundles software that includes the cloud ERP, process intelligence and execution, advanced office of the CFO features, and more, along with a complete cloud infrastructure and migration services.

Source: https://www.sap.com/africa/products/erp/rise.html

Claim 1	Identification



Source: https://www.amd.com/system/files/documents/AMD-EPYC-7002-Series-Datasheet.pdf; *see also* https://www.amd.com/en/processors/epyc-7002-series.



Claim 1	Identification
	Source: https://www.amd.com/system/files/documents/amd-epyc-7003-series-datasheet.pdf; *see also* https://www.amd.com/en/processors/epyc-7003-series.  Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

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	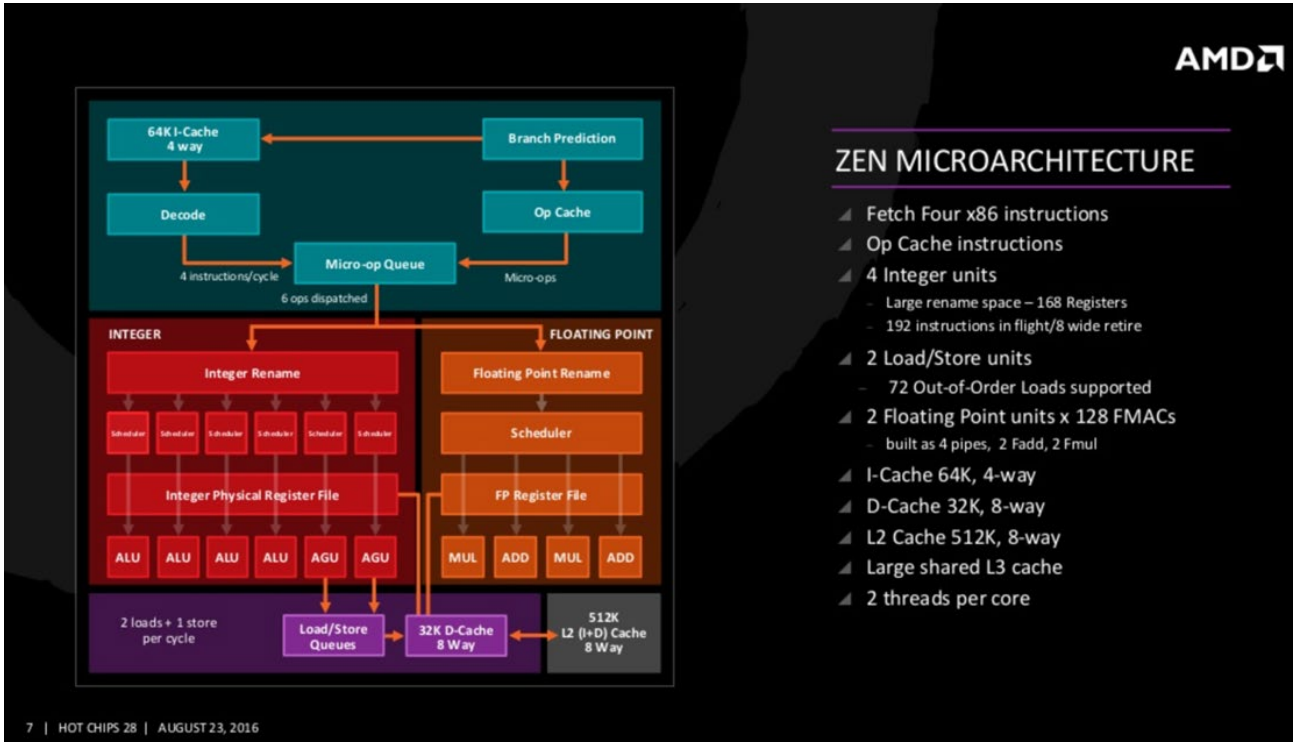 Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https://www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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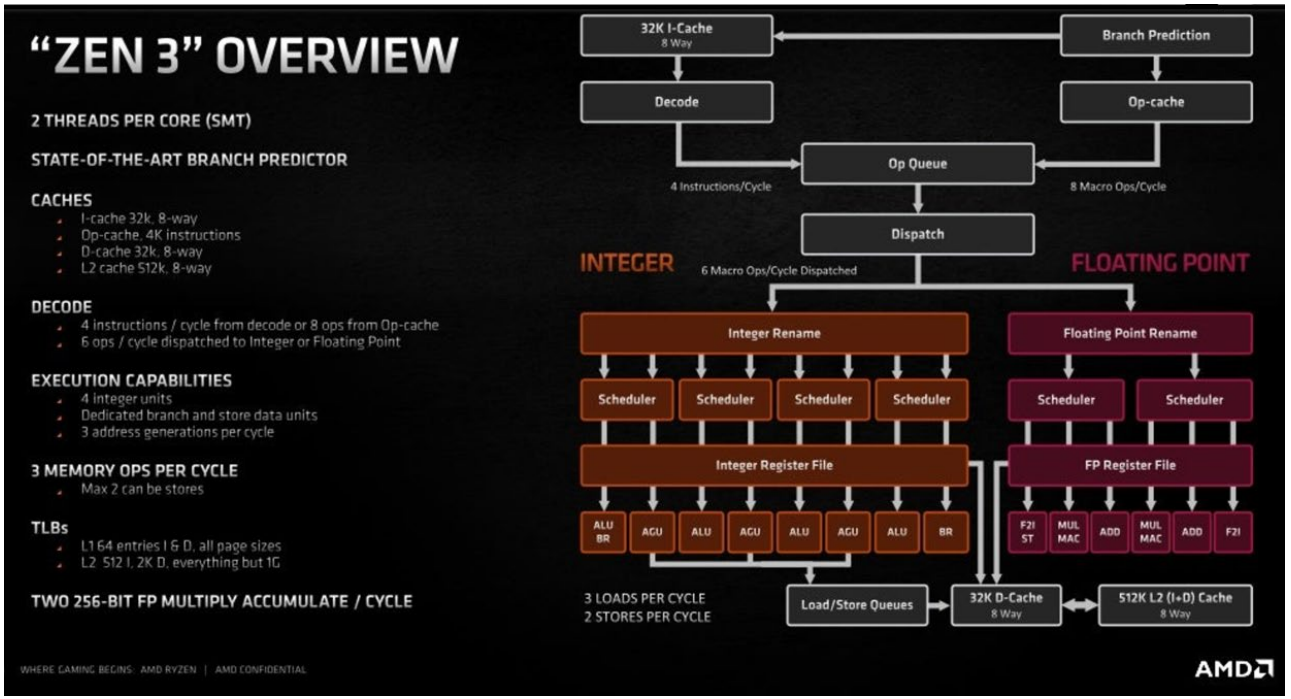
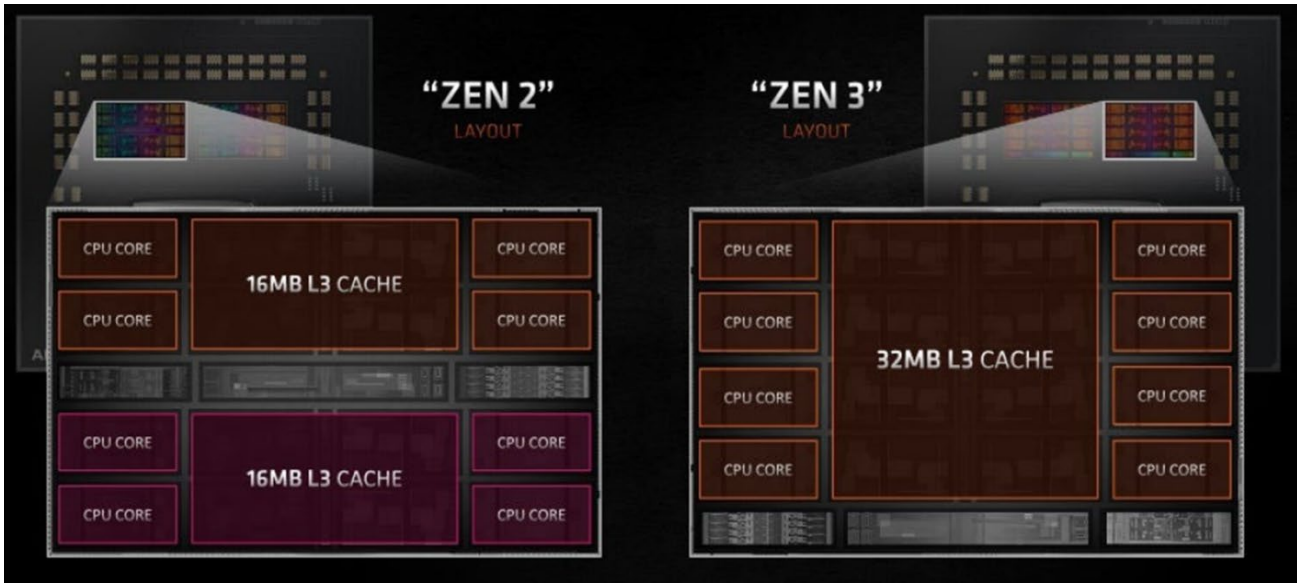
	 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

Claim 1	Identification
1[a]. a first processor, coupled to fetch instructions and access data through a first cache controller;	SAP provides a first processor, coupled to fetch instructions and access data through a first cache controller. For example, *see*:  Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

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	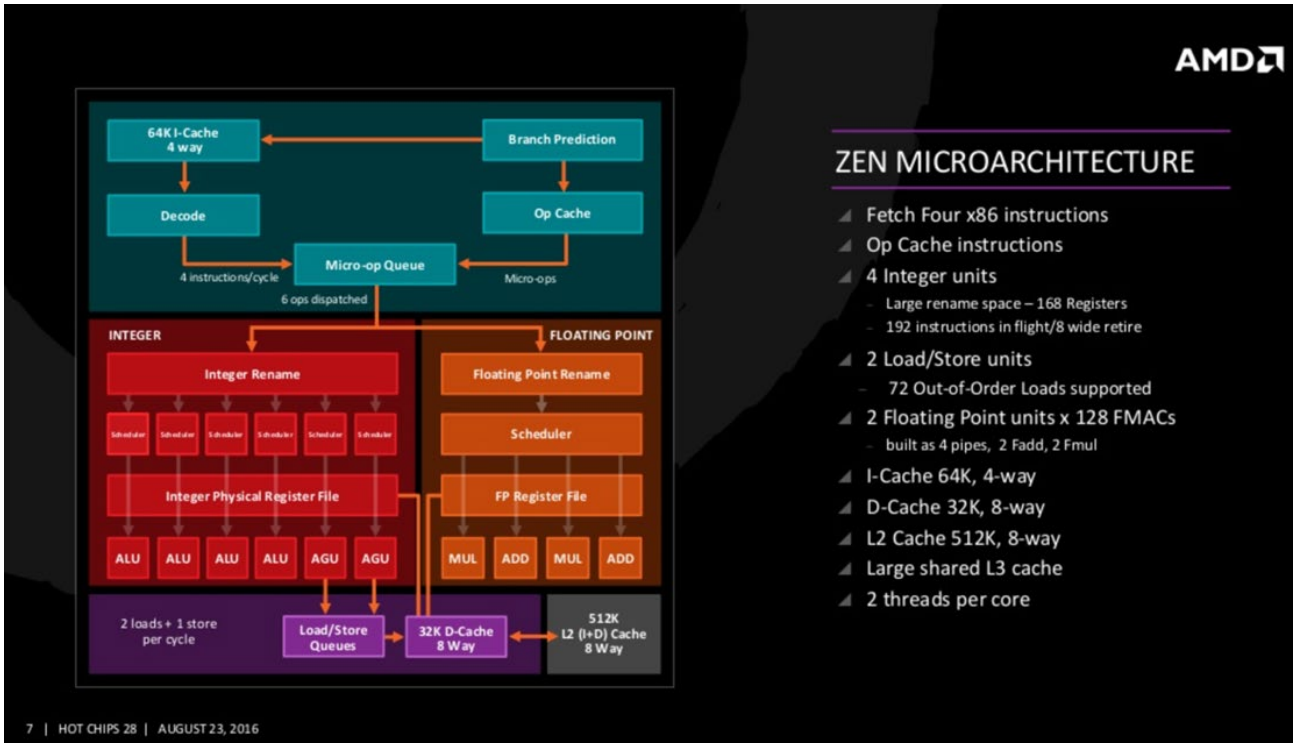 Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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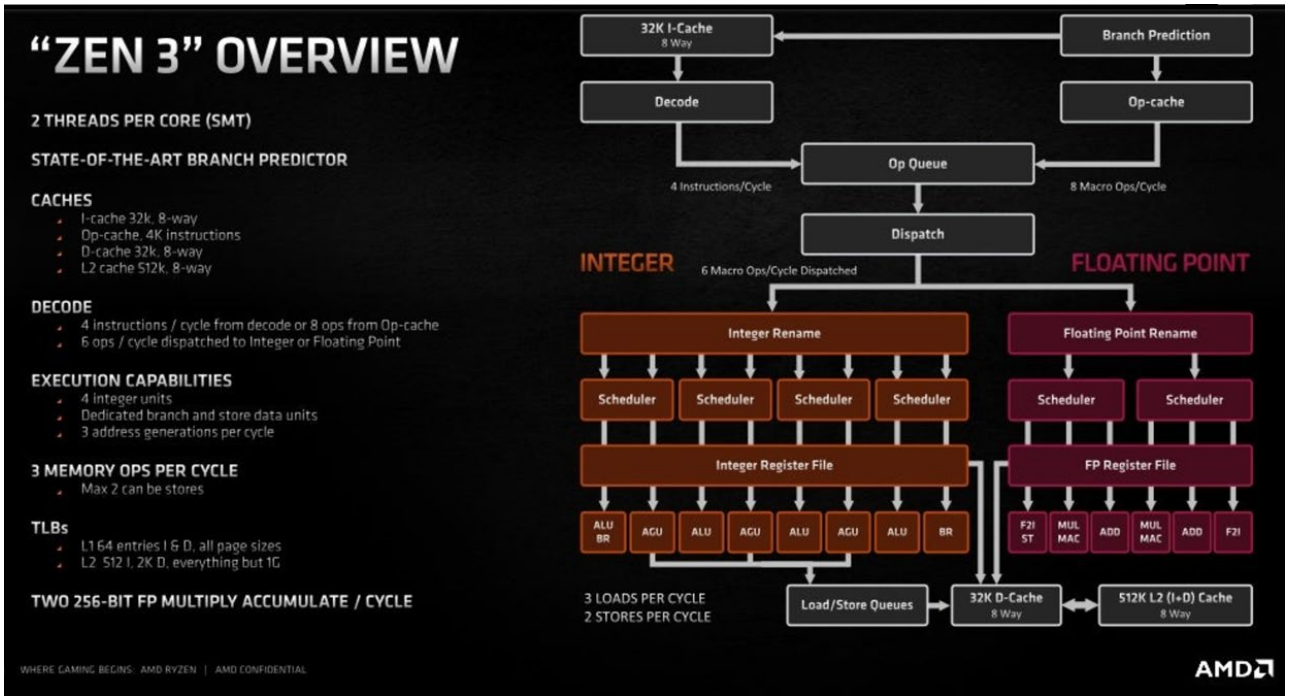
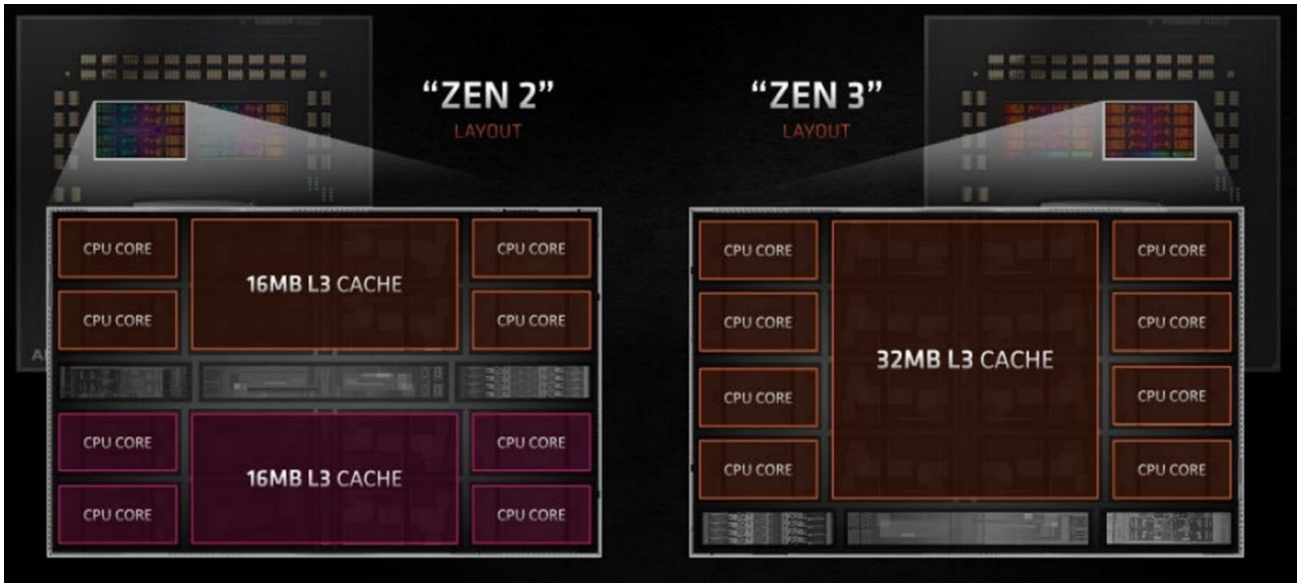
	 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

Claim 1	Identification
1[b]. a second processor, coupled to fetch instructions and access data through a second cache controller;	SAP provides a second processor, coupled to fetch instructions and access data through a second cache controller. For example, *see*:  Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

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	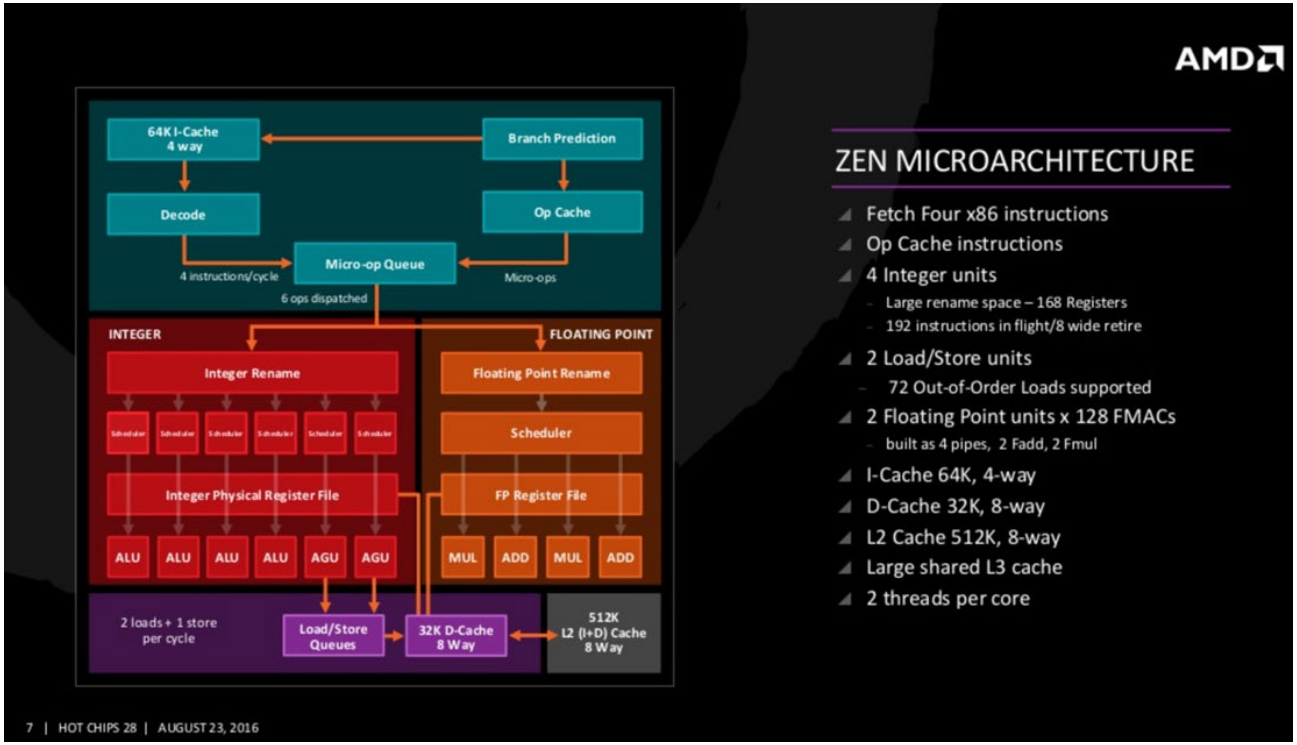 Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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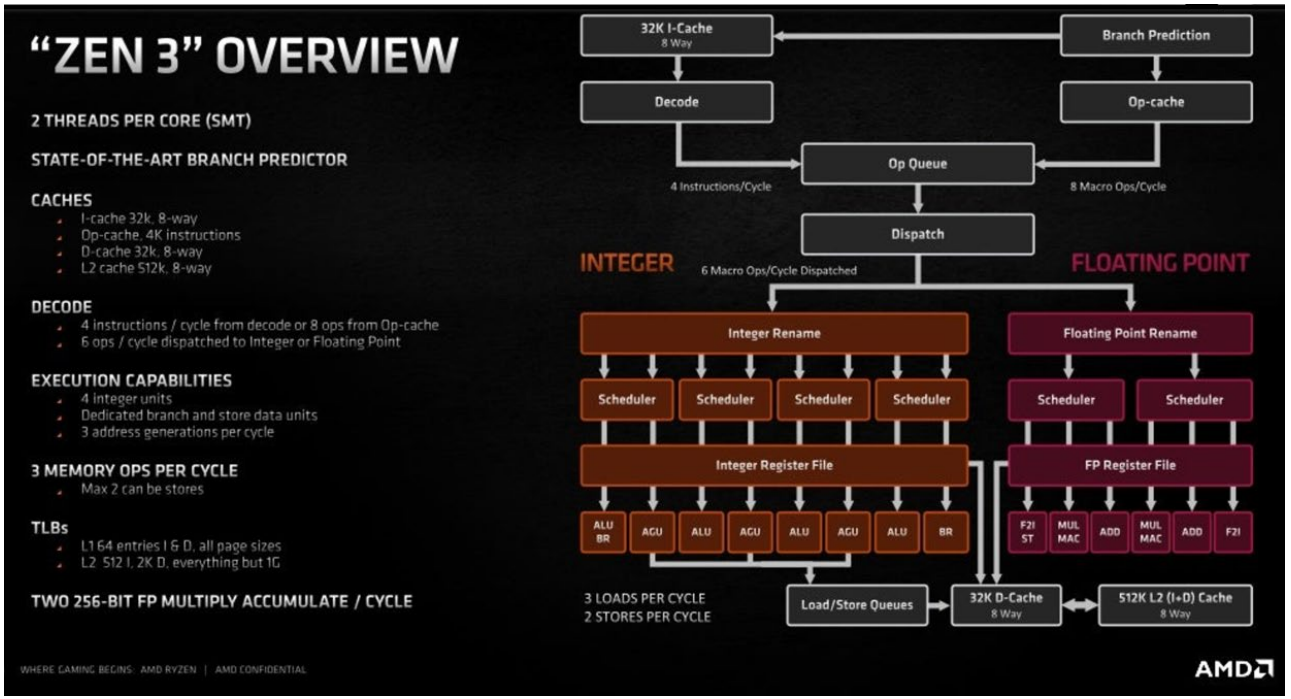
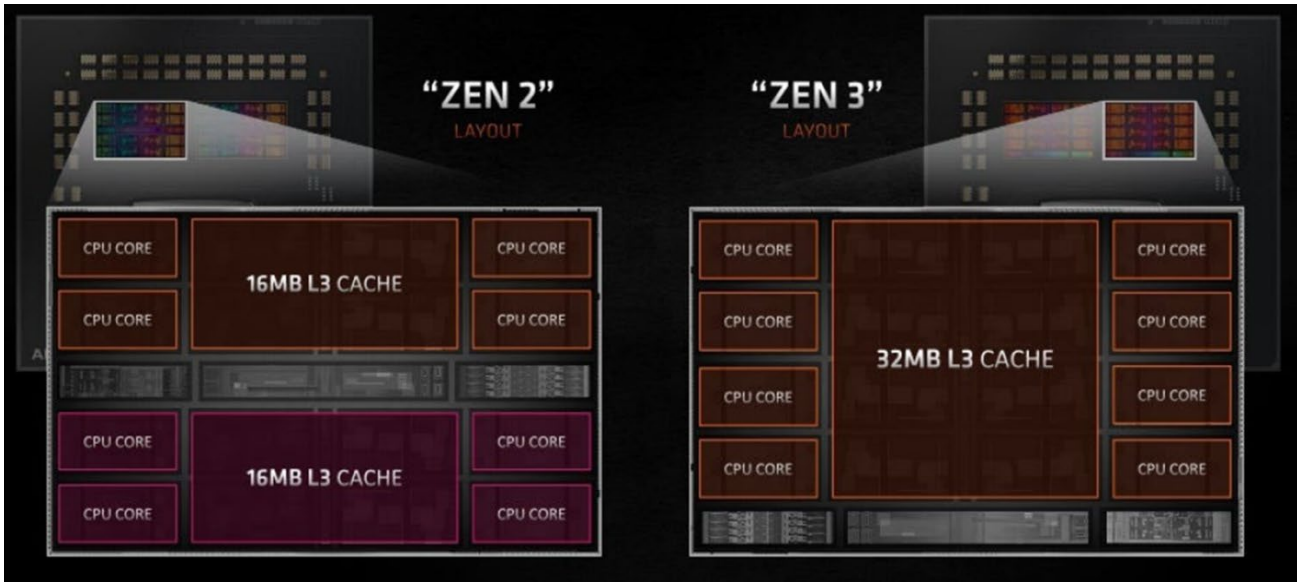
	 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

Claim 1	Identification
1[c]. a plurality of cache memory blocks;	SAP provides a plurality of cache memory blocks. For example, *see*:  Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

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	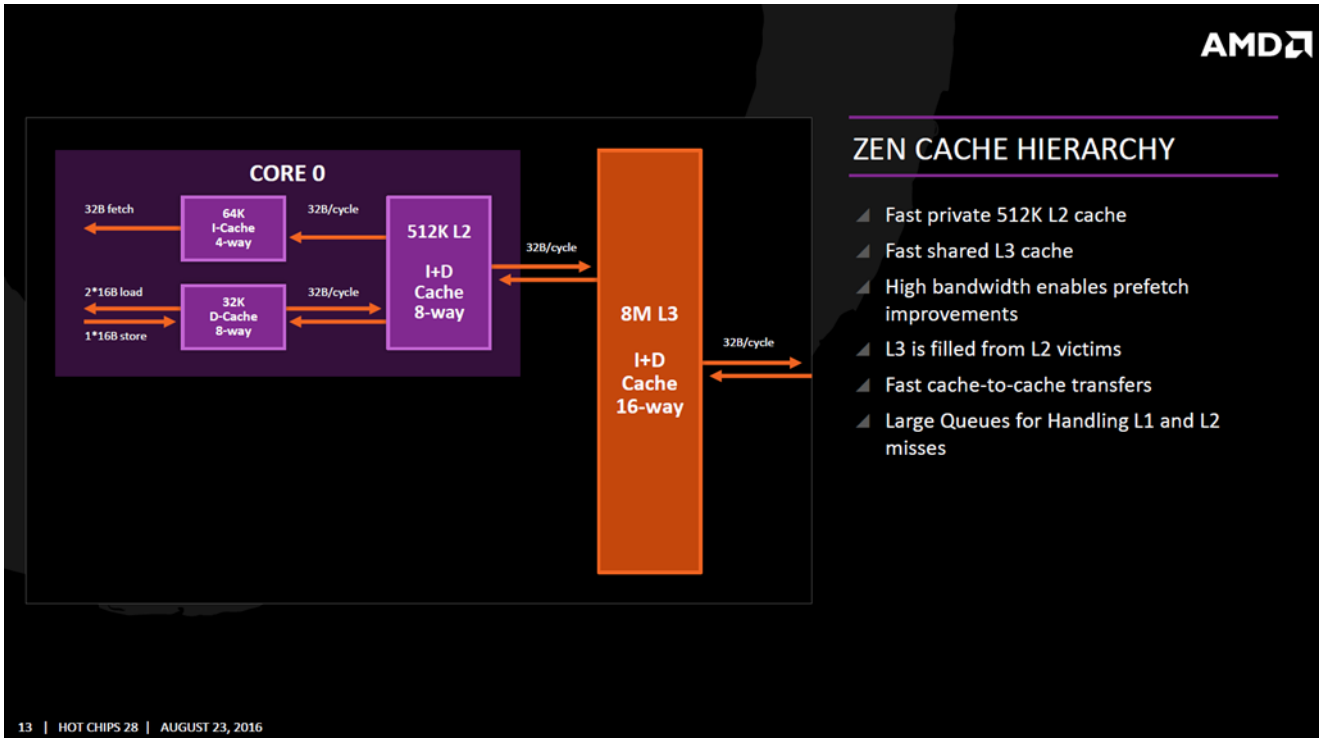 Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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	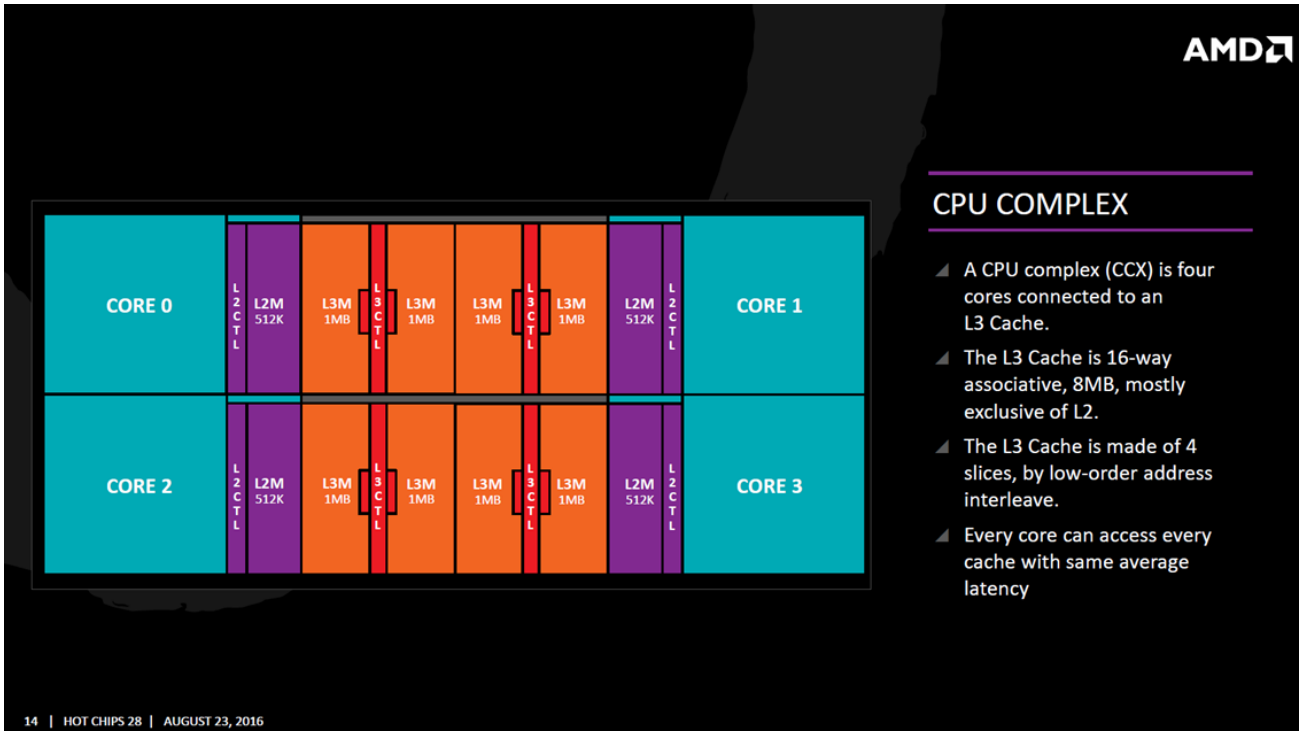 Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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	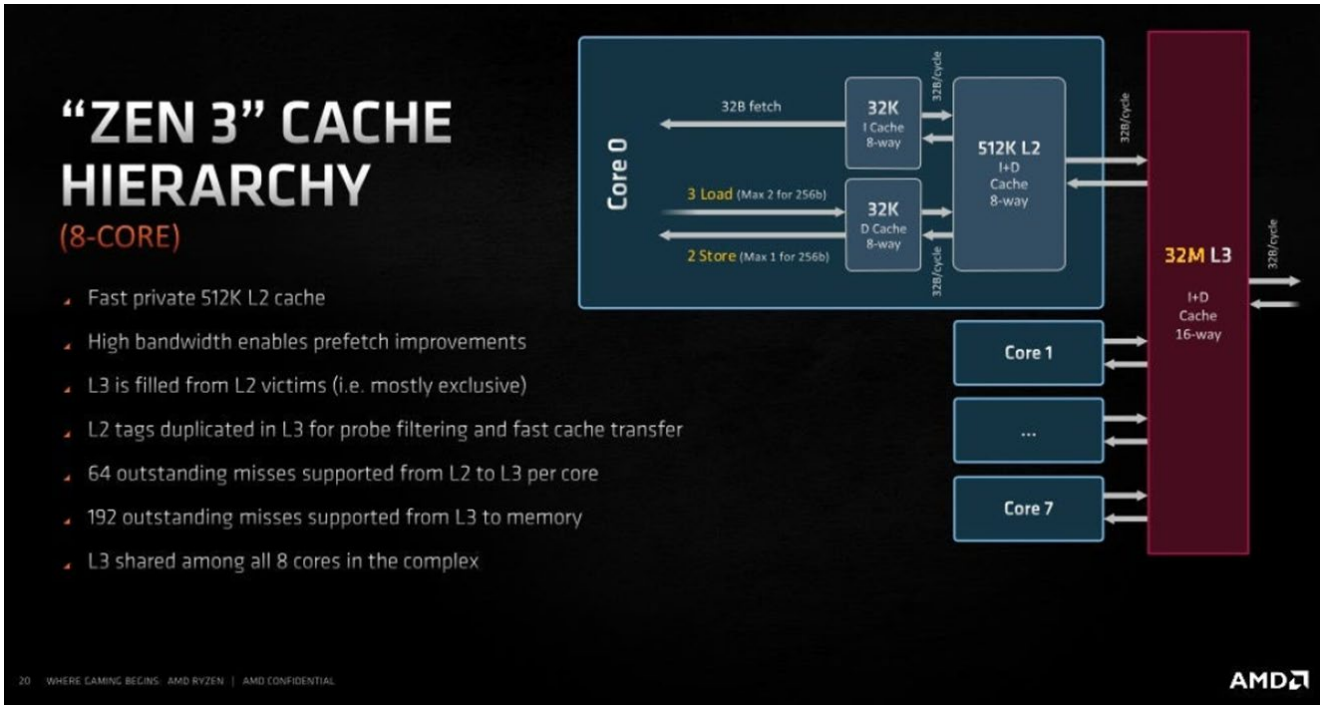 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

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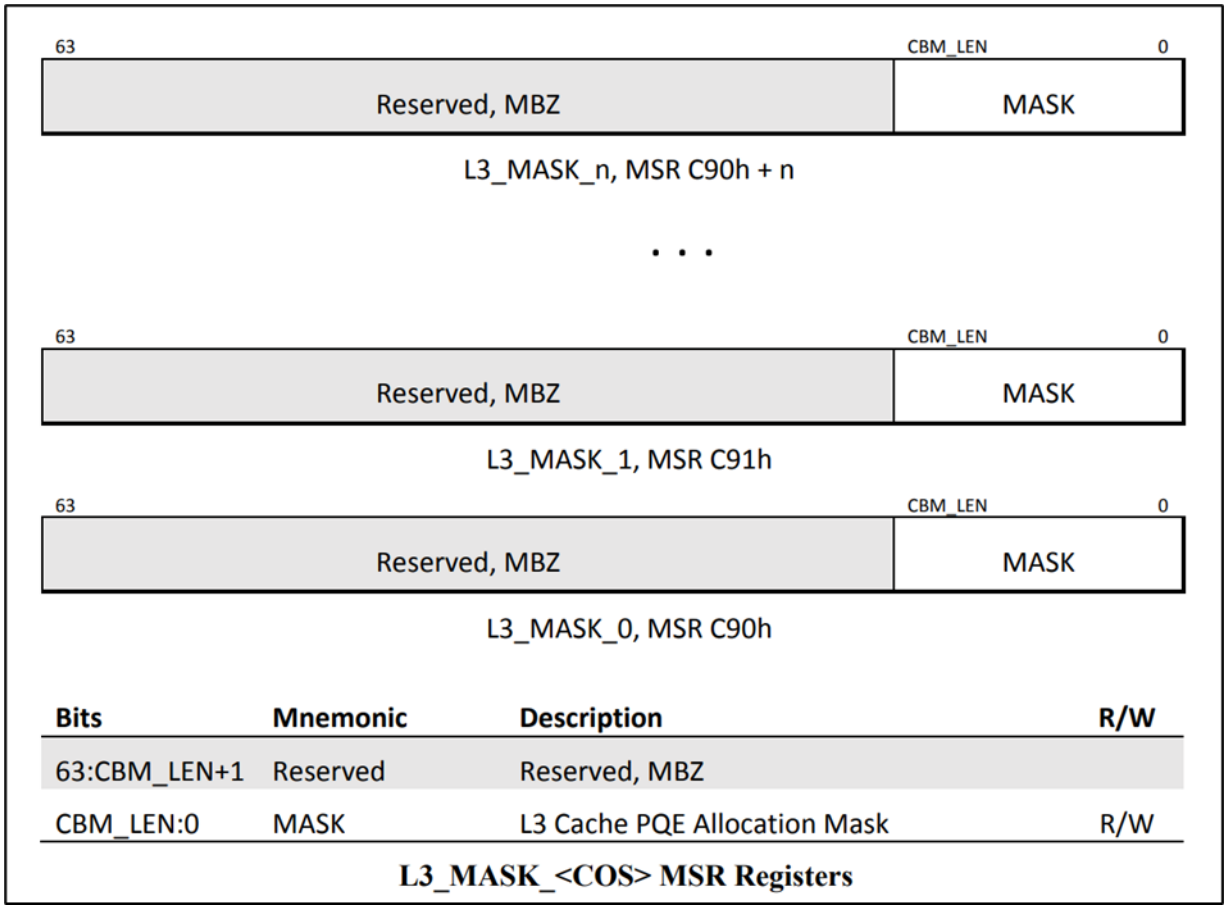
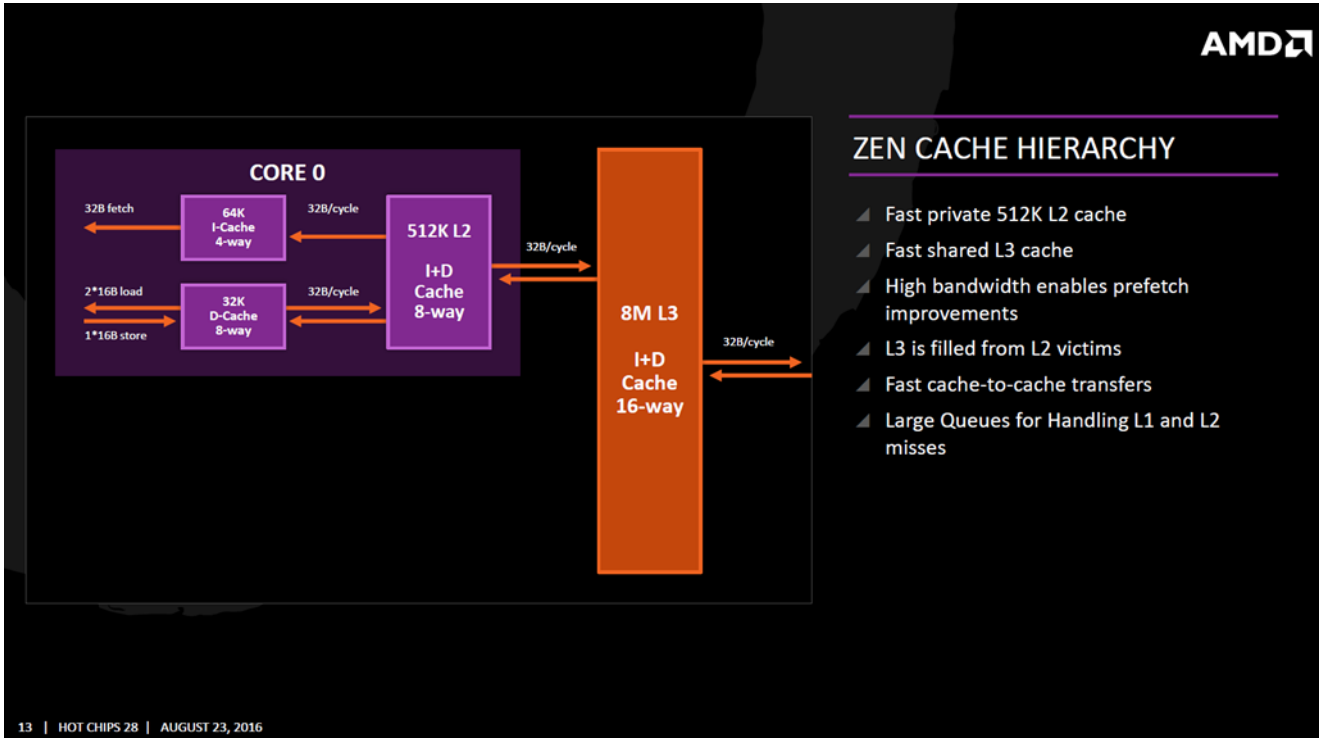


Bits	Mnemonic	Description	R/W
63:CBM_LEN+1	Reserved	Reserved, MBZ	
CBM_LEN:0	MASK	L3 Cache PQE Allocation Mask	R/W

L3_MASK_<COS> MSR Registers

Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf

Claim 1	Identification
1[d]. a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers; and	SAP provides a high-speed interconnect coupling the plurality of cache memory blocks to the first and second cache controllers such that at least one allocable cache memory block is capable of being used by the first and second cache controllers. For example, *see*:  Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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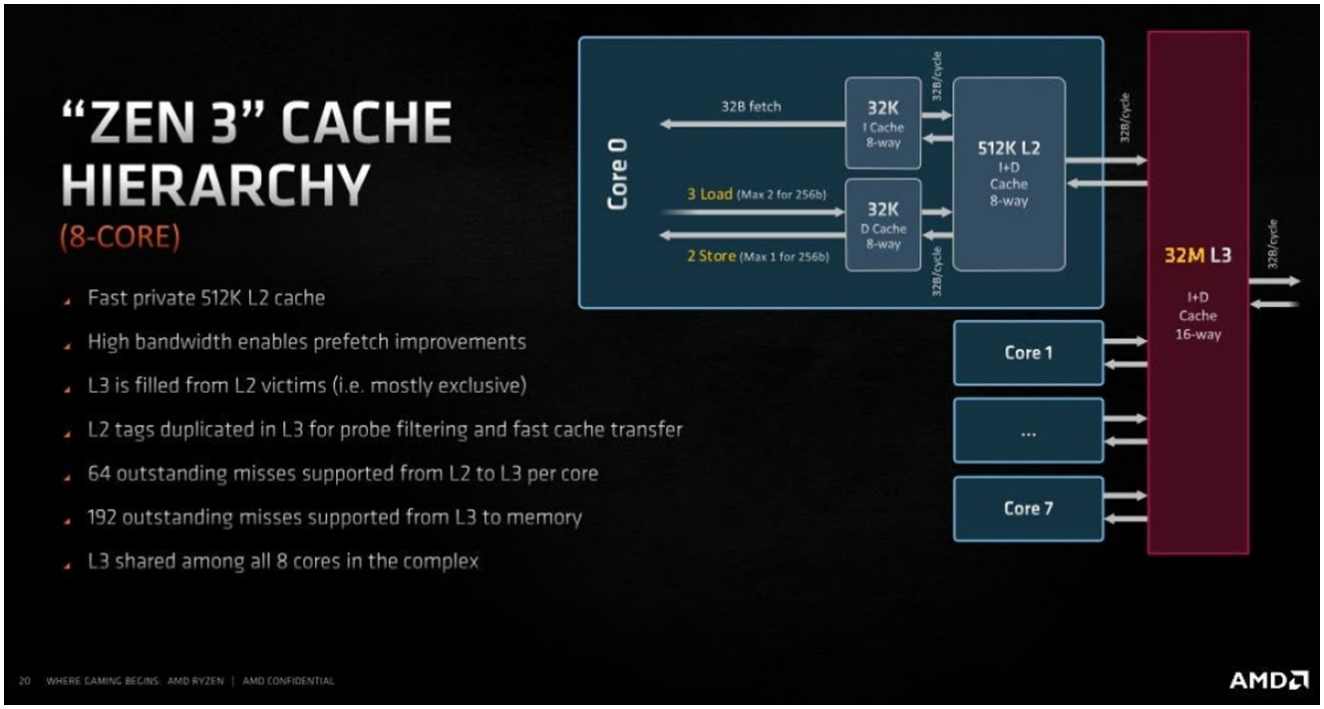
	 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

Claim 1	Identification

QOS Enforcement

QOS enforcement is accomplished by assigning a Class Of Service (COS) to a processor and specifying allocations or limits for that COS for each resource to be allocated. The current COS for a given processor is specified in the PQR_ASSOC MSR, described above. If multiple processors within a QOS domain are assigned the same COS, then the resource allocation associated with that class will be shared among all the processors. At reset, the PQR_ASSOC.COS value is 0.

For each resource which is managed by the Platform QOS Enforcement feature, a bank of registers is defined which software can program with the allocation limits for each COS. The interpretation of that register depends on the type of resource which is being managed.

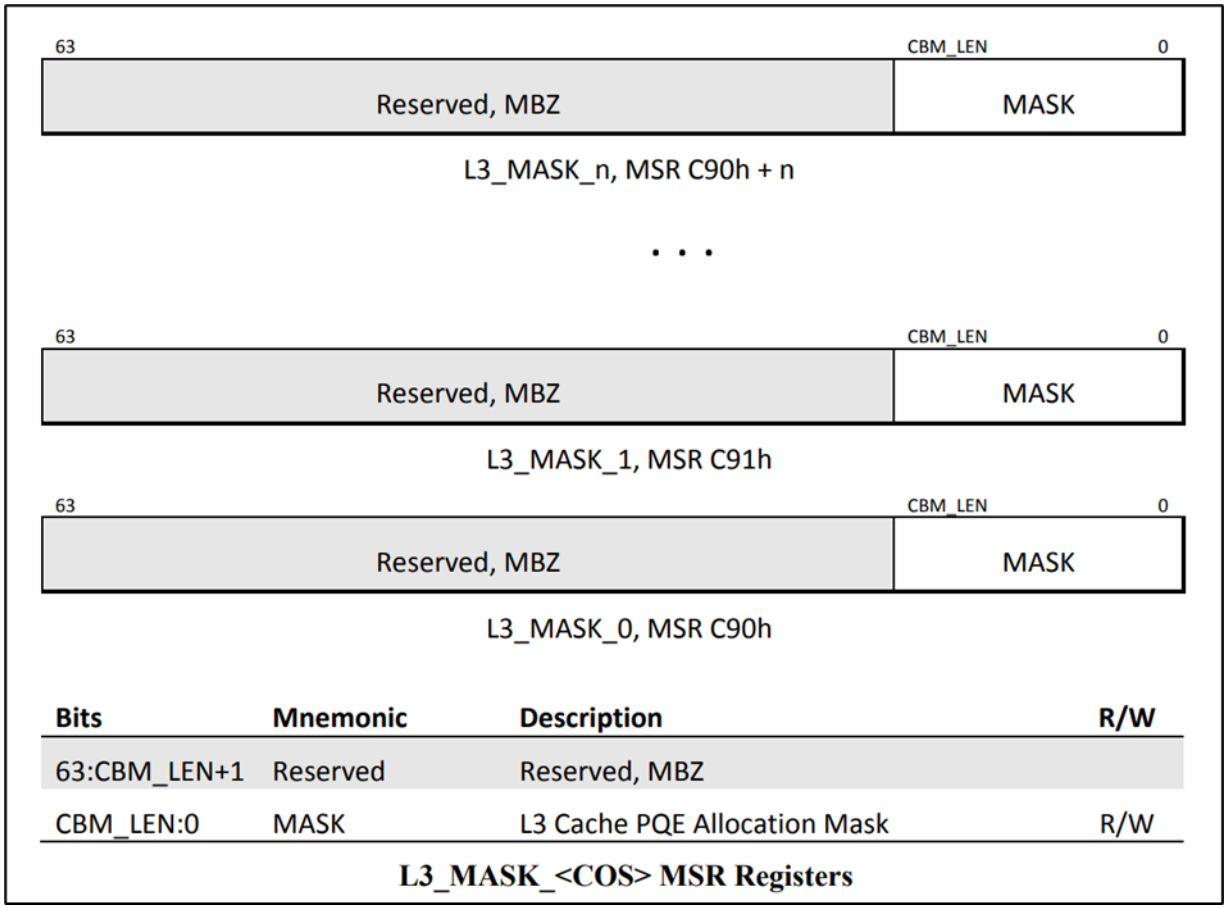
Platform QOS Limits for Cache Allocation Enforcement

The PQE limits for L3 cache allocation are specified by a bank of MSRs called L3_MASK_n, where "n" is the COS. These registers begin with MSR C90h. There is one register for each COS implemented for that resource. Each of the registers is a bitmask with the MSB at CBM_LEN, which is returned in EAX[4:0] by CPUID Fn0000_0010, EAX=1. (This length is zero-based, so the actual number of QOS bits is EAX[4:0] + 1).

Software programs these registers with a bit mask where each "1" represents a portion of the cache which may be used by the corresponding COS. For example, if CBM_LEN for a given implementation is 15, then each "1" which is set in L3_MASK_n represents 1/16 of the cache which may be used by processors running with COS = n. If two or more different Classes of Service have a "1" set in the same bit position in their respective L3_MASK_n register, that represents a portion of the cache which is competitively shared by processors running with those COS values. Some products may implement Cache Allocation Enforcement by allocating some number of ways of the L3 cache for each "1" in the L3_MASK register, but this will not necessarily be true for all implementations and software should not rely on that interpretation.

However, because this is one possible implementation, it is possible that use of PQE for cache allocation will reduce the effective associativity available to processes running using an L3_MASK which does not have all the bits set. The bits which are set in the various L3_MASK_n registers do not have to be contiguous and may overlap in any desired combination. If an L3_MASK_n register is programmed with all 0's, that COS will be prevented from allocating any lines in the L3 cache. At reset, all L3_MASK_n registers are initialized to all 1's, allowing all processors to use the entire L3 cache accessible to them.

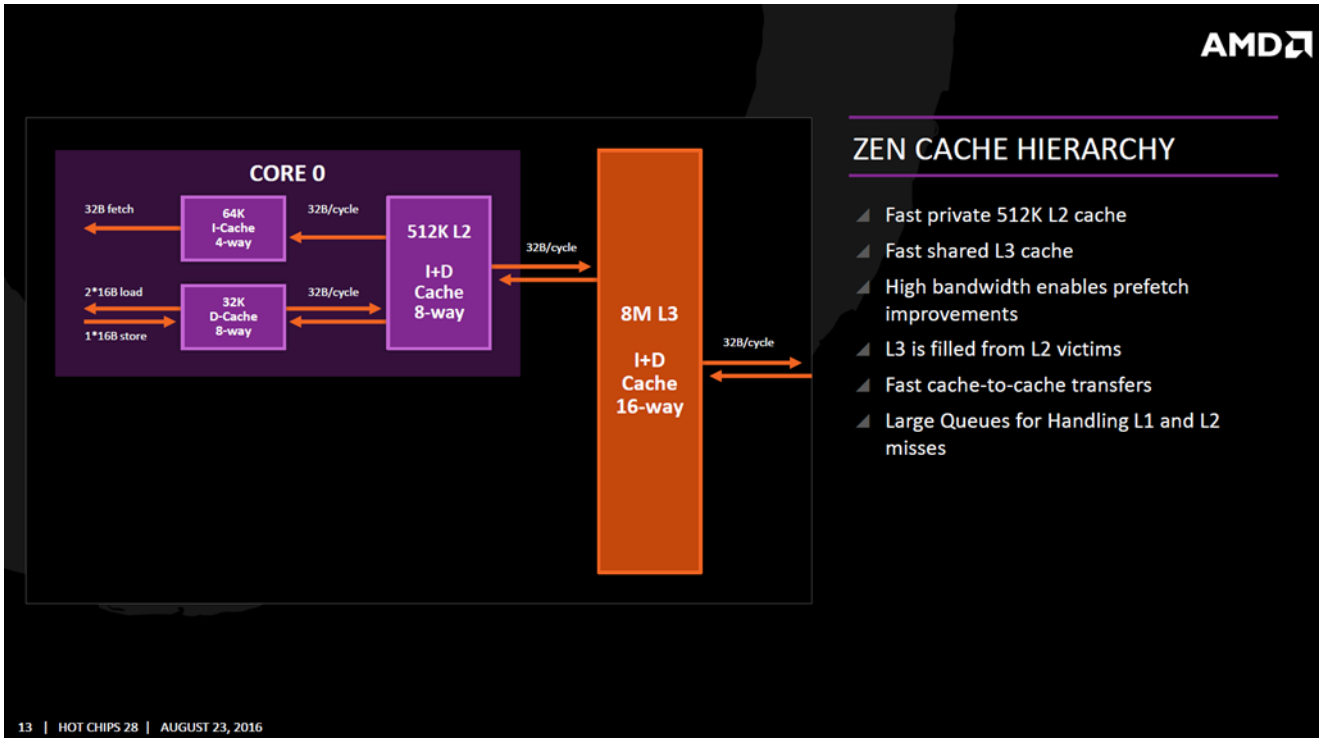
Claim 1	Identification
	Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf



Bits	Mnemonic	Description	R/W
63:CBM_LEN+1	Reserved	Reserved, MBZ	
CBM_LEN:0	MASK	L3 Cache PQE Allocation Mask	R/W

L3_MASK_<COS> MSR Registers

Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf

Claim 1	Identification
1[e]. a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, whereby the accessing cache memory controller is allowed to access the allocable cache memory block,	SAP provides a resource allocation controller coupled to determine an accessing cache memory controller selected from the group consisting of the first and second cache memory controllers, whereby the accessing cache memory controller is allowed to access the allocable cache memory block. For example, *see*:  Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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	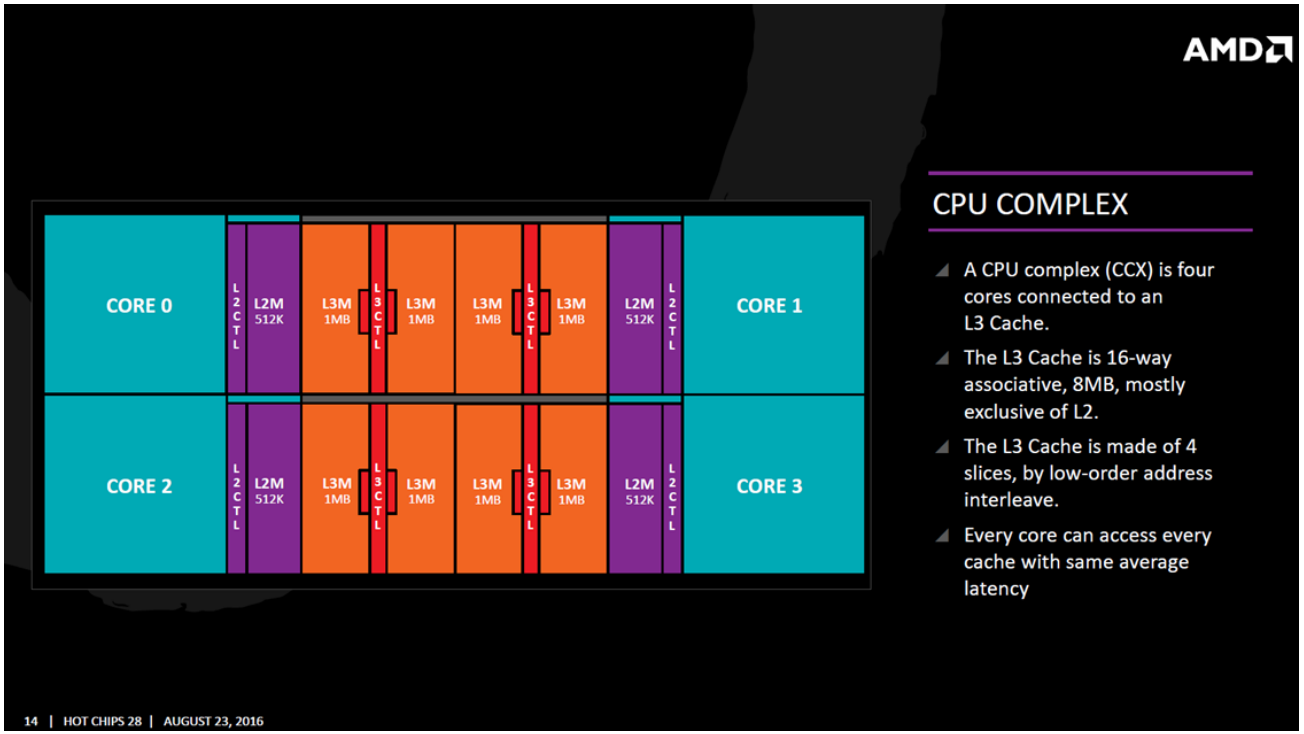 Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

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	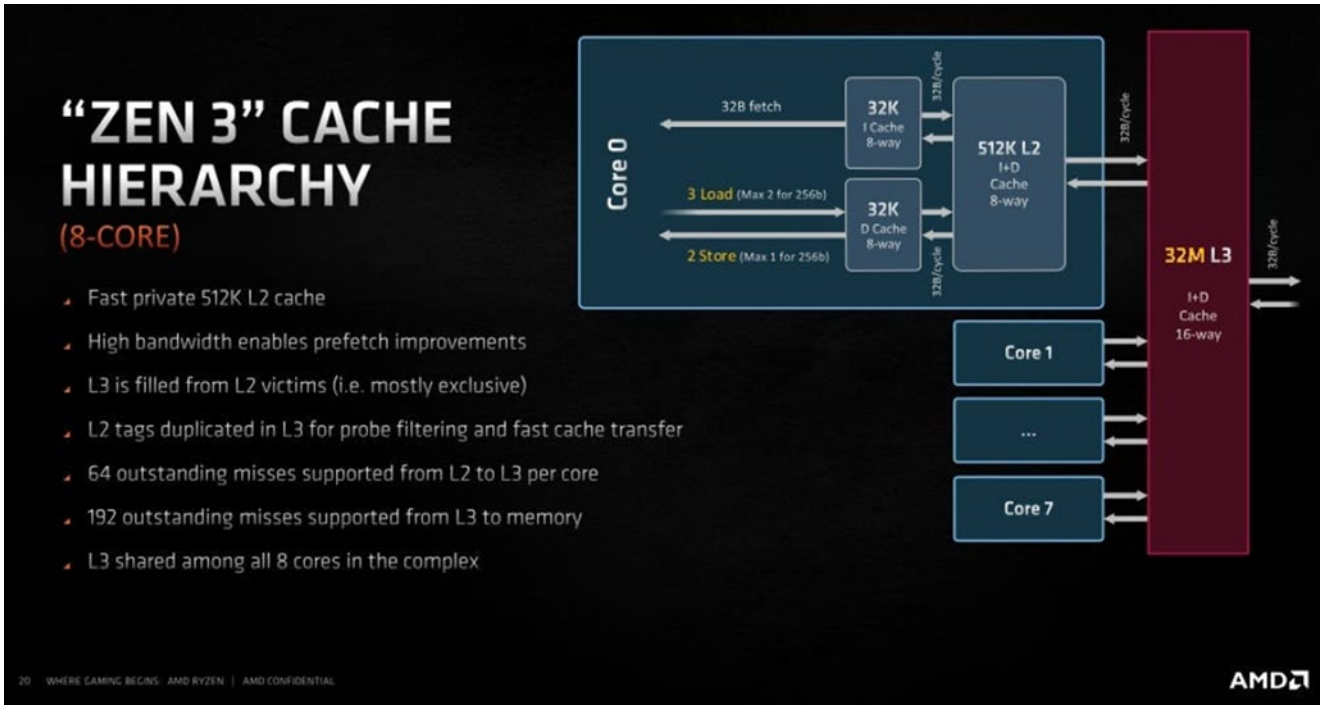 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

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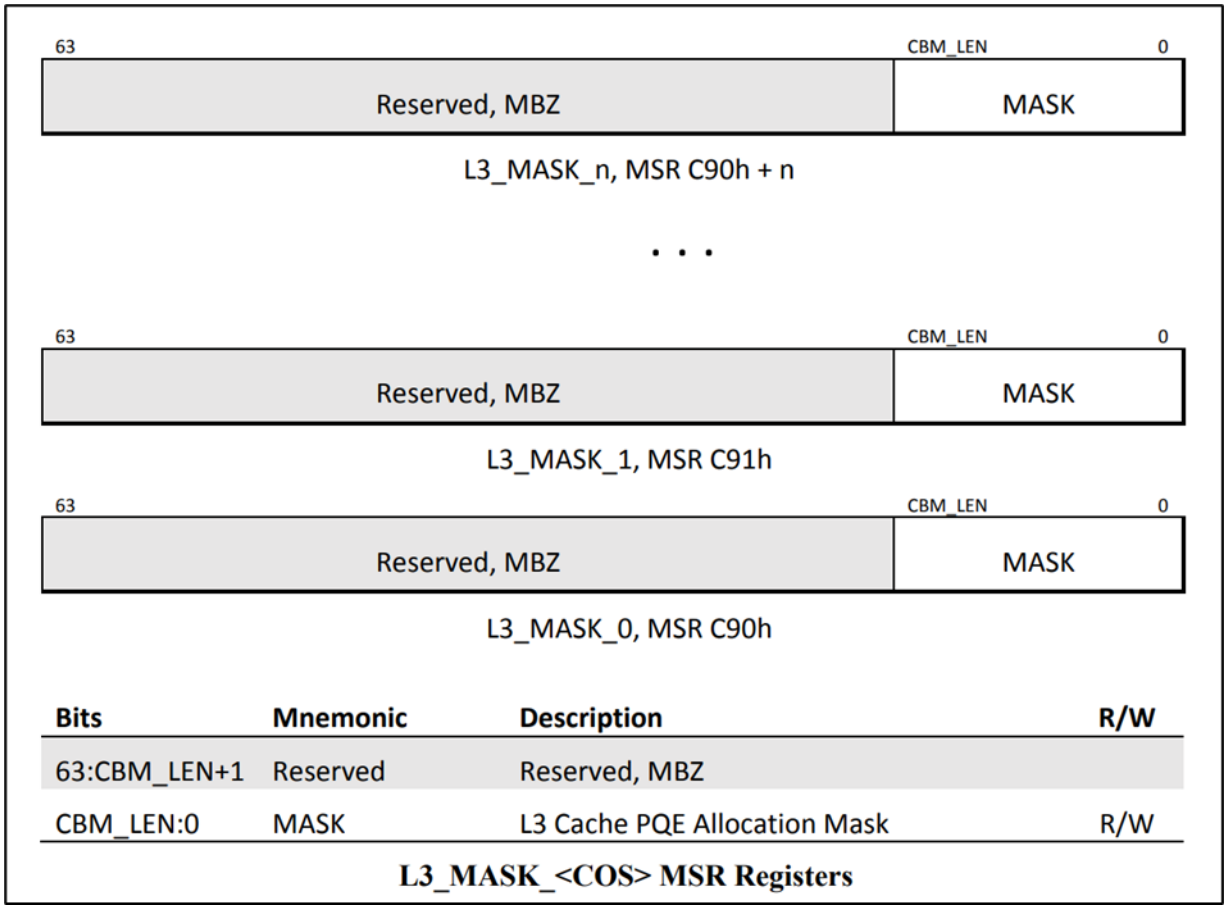

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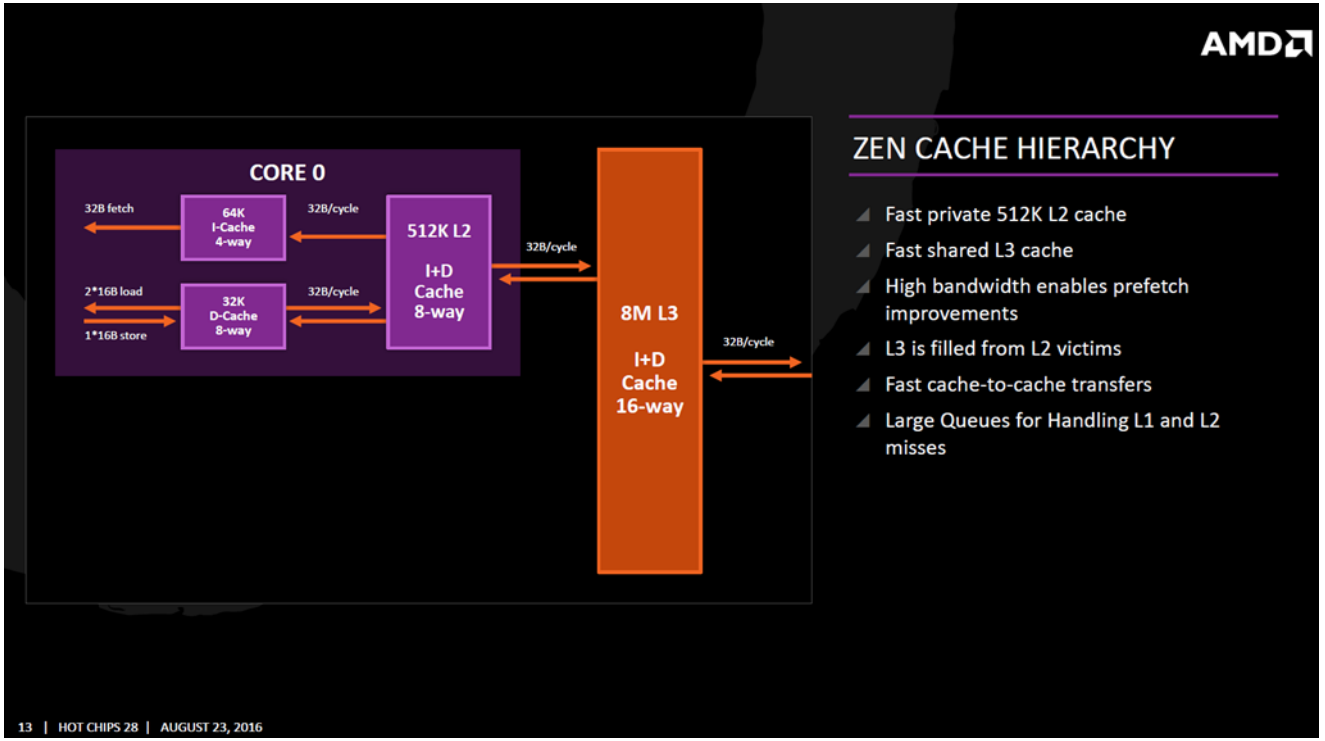
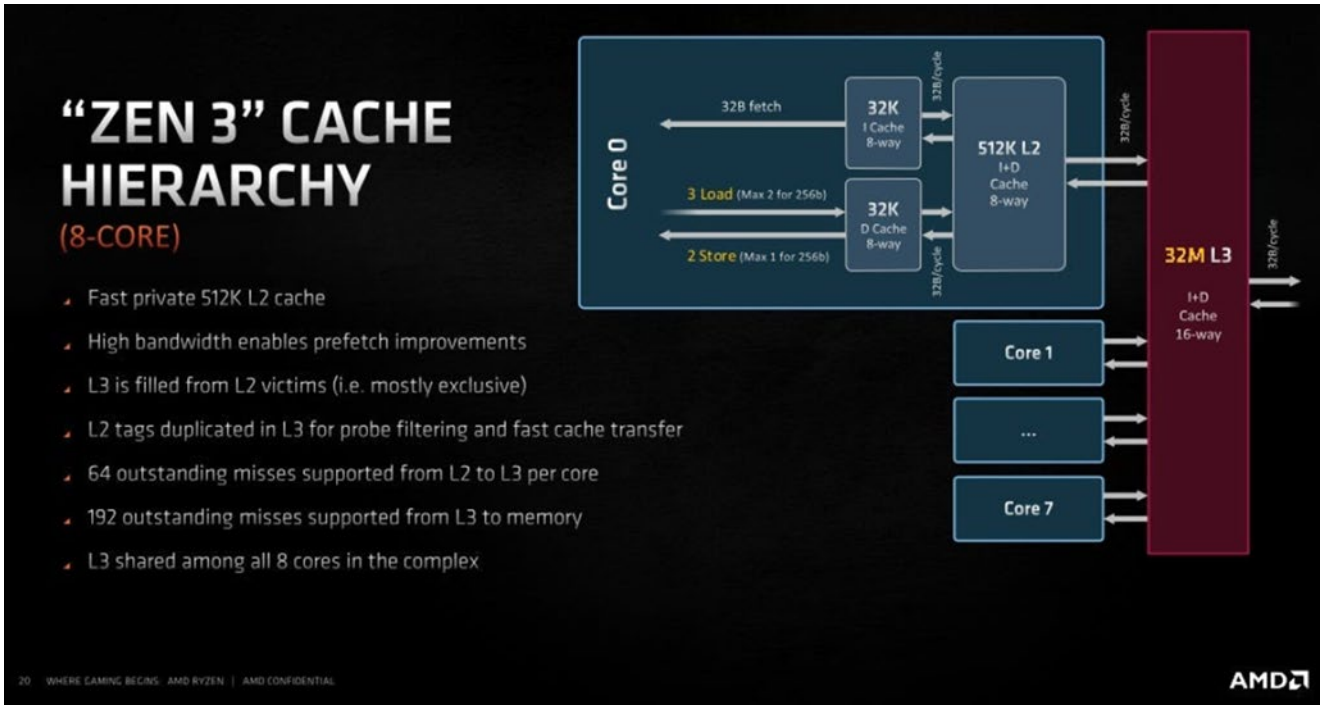
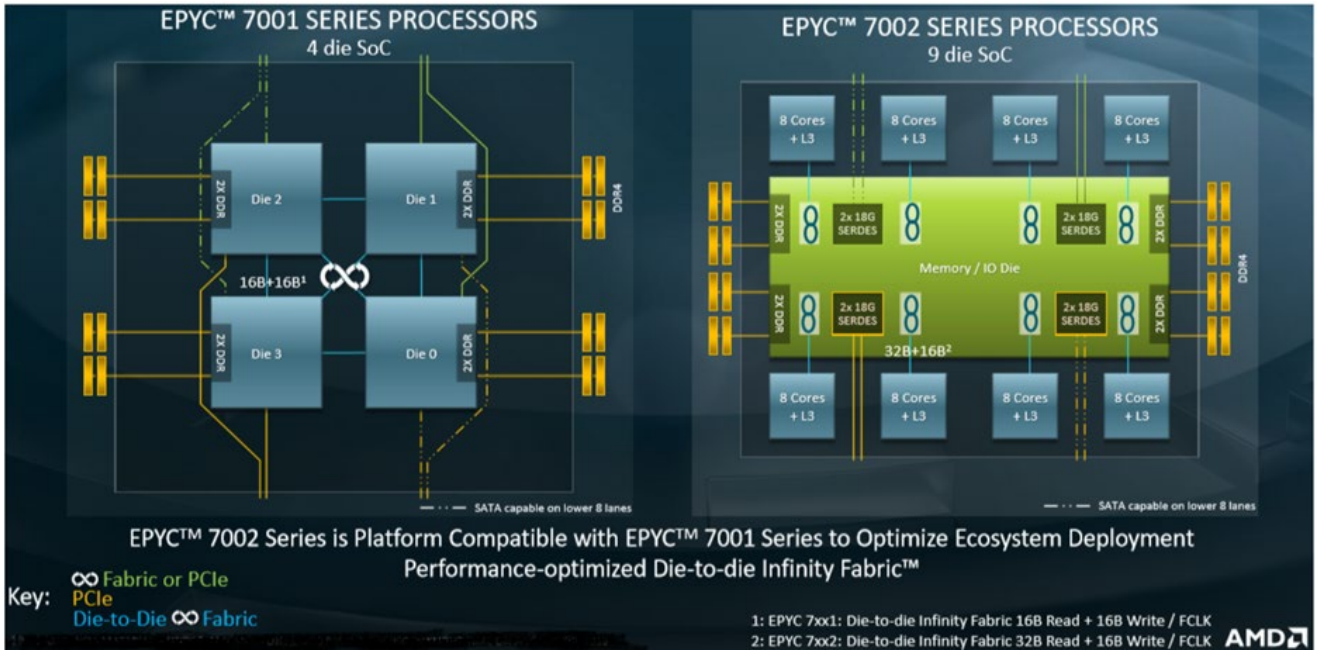
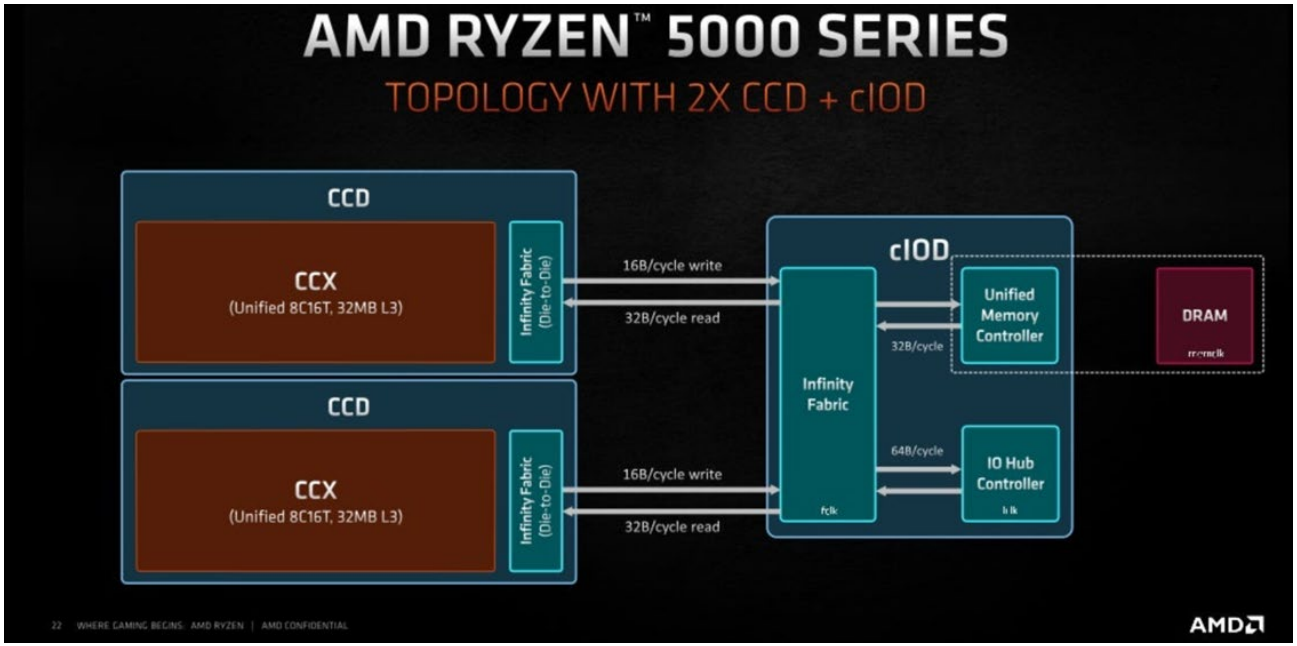
L3_MASK_<COS> MSR Registers

Source: https://web.archive.org/web/20210305161038/https://developer.amd.com/wp-content/resources/56375_1.00.pdf

Claim 1	Identification
1[f]. wherein the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random-access memory.	SAP provides the resource allocation controller wherein the cache memory blocks are usable by the cache controllers to store data and instructions fetched from a random-access memory. For example, *see*:  Source: https://docplayer.net/34910004-A-new-x86-core-architecture-for-the-next-generation-of-computing.html; *see* https://web.archive.org/web/20190611023103/https://www.amd.com/en/technologies/zen-core; https://web.archive.org/web/20190430213825/https:// www.slideshare.net/AMD/amd-and-the-new-zen-high-performance-x86-core-at-hot-chips-28.

Claim 1	Identification
	 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.

Claim 1	Identification
	 Source: https://www.nextplatform.com/2019/08/15/a-deep-dive-into-amds-rome-epyc-architecture/

Claim 1	Identification
	 Source: https://web.archive.org/web/20220903163656/https://www.slideshare.net/slideshow/embed_code/key/6g7kfAYmt73ofd; *see also* https://web.archive.org/web/20220903163610/https://www.amd.com/en/technologies/zen-core-3.